Application No.09/630,258
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REMARKS

Reconsideration of the application, as amended, is respectfully requested. All objections and rejections are respectfully traversed.

Claims 1-8 are rejected under 35 USC § 112, second paragraph, as being indefinite with regard to the subject matter the Applicant regards as the invention. In particular, the Examiner objects to the use of the term "the order calculated." The Applicant has amended claims 1, 5, and 8 to more clearly state that the output data is stored in sequential memory locations not just in any order calculated, but rather the data is stored in sequential memory locations in the order that the data are used in the calculations in the next stage.

Claims 1-8 are pending in the instant application and stand rejected as being anticipated by Nakai et al., ("Nakai"). In the Official Action, the Examiner posits that Fig. 7 of Nakai discloses an FFT processing [i+2] wherein the symbol input is input into the RAM in the time order x(0) to x(7), and that the claim language does not clearly disclose a particular order for storing the output in a third memory.

The Applicant respectfully submits that the Examiner may have misunderstood the use of the term "unity stride" in the current application, and therefore respectfully traverses the rejection. The Applicant respectfully points out that on page 8, lines 3-20, the application states:

> FFT calculation stage 208 calculates output data values 206. These output data values are stored sequentially in a third memory area 212, in the order in which they are calculated. As will be explained in detail below, this ordering and storing of the

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> output data values in the order of calculation provides for unity stride memory operations for the output data values.

Moreover, on page 10 line 13 the Applicant defines the term "in the order calculated refers to":

> The first butterfly calculator uses the input data x(0) and x(4). The output data values from this FFT butterfly are stored in the first and second memory locations 310, 312. The second butterfly calculator uses the input data x(1) and x(5). The output data values from this FFT butterfly are stored in the third and fourth memory locations 314, 316. The third butterfly calculator uses the input data x(2) and x(6). The output data values from this FFT butterfly are stored in the fifth and sixth memory locations 318, 320. The fourth butterfly calculator uses the input data x(3) and x(7). The output data values from this FFT butterfly are stored in the seventh and eighth memory locations 322, 324. Thus, the output data values are "re-ordered" according to the calculation order, unlike the traditional FFT algorithm illustrated in Fig.1.

In addition, Fig. 6 in the present application depicts a three-stage FFT architecture in accordance with the present invention. In particular, the description accompanying Fig. 6 on page 12 line 23-page 13 line 2 states:

> In addition in the presently disclosed FFT method, the input data 608 is not re-ordered, and the output data values for each stage are properly ordered by the use of the unity stride memory operations discussed above. Thus, the re-ordering that is necessary in the traditional FFT method is eliminated, along with, the additional

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> memory read/write operations. The decrease in the complexity of the calculations needed for the memory read/write operations improves the efficiency of the operation of the presently disclosed method over the traditional FFT methods as well.

The Applicant asserts therefore, that the specification makes clear that the input data to each stage is not re-ordered, i.e., that the data is read from memory in the order that the data is stored in the memory. Thus, the term "unity stride" should be understood to mean that the data from the previous stage is written into memory locations of the third memory such that the data is ordered in memory in the same order in which the data is used in the calculations in the next stage as depicted in Figs. 3 and 6 and described above.

The Applicant therefore believes that the claims as amended after the first office action were patentably distinct over the Nakai reference. However, in order to further clarify this distinction, claims 1, 5, and 8 have been amended to further clarify the definition of the unity stride term as it is defined in the specification and used in the claims. Claim 1, which can be used as an exemplar for the other amended claims, states: "(f) storing said R butterfly output data values in sequential memory locations of a third memory in the order in which the output data values are used in the calculations in a next stage."
Additionally clarifying amendments to the claims have been made.

In contrast to the claimed invention, Nakai in Fig. 7 teaches that the symbol output of the FFT processing [i], [i+2], and [i+4] stages is not in the order that the subsequent stage uses the symbol input. The symbol output is stored in the order calculated

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by the preceding stage and is then used by the subsequent stage in a different symbol order than is stored in memory. Thus unlike the claimed invention, the symbol output data are not used by the subsequent FFT processing stage in the order that they are stored.

For the reasons set forth above, the Applicant asserts that independent claims 1, 5, and 8 are patentably distinct over the Nakai reference and the Applicant respectfully requests the reconsideration and allowance of these claims. Claims 2-4 and 6-7 depend from claims 1 and 5 respectively and are believed to be patentable for at least the same reasons as claims 1 and 5.

In view of the foregoing remarks and amendments, the Applicants respectfully submit that all present claims and the Application are in condition for allowance and such action is respectfully solicited.

The Examiner is encouraged to telephone the undersigned attorney to discuss any matter which would expedite allowance of the present application.

Respectfully submitted,

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